DESCRIPTION

The A24S128 provides 131,072 bits of serial electrically erasable and programmable read only memory (EEPROM), organized as 16,384 words of 8 bits each.

The A24S128 is cascadable feature allows up to 4 devices to share a common 2-wire bus.

The A24S128 is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential.

The A24S128 is access via a 2-wire serial interface from 1.7 to 3.6V.

The A24S128 is available in CSP4 package.

ORDERING INFORMATION

Package Type	Part Number	
CSP4 SPQ: 5,000pcs/Reel	G4	A24S128G4R-XXZ
		A24S128G4VR-XXZ
Note	XX: Address Code Please see Address Table Z: Package Type A: Ball Pitch 0.4mm x 0.5mm B: Ball Pitch 0.4mm x 0.4mm V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

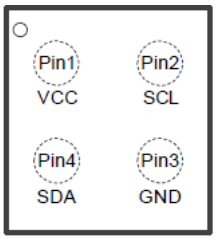
FEATURES

- Single supply voltage and high speed:
  - 1MHz@1.8V
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional data transfer protocol
- Memory array:
  - 128 Kbits (8 Kbytes) of EEPROM
  - Page size: 64 bytes
- Random and sequential Read modes
- Write:
  - Byte Write within 3 ms
  - Page Write within 3 ms
  - Partial Page Writes Allowed
- Software data Protection
- Slave Address Configurable
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
- Available in CSP4 package

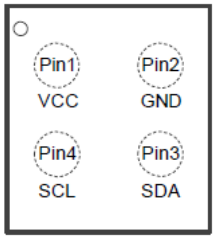
ADDRESS TABLE

Address Code	A2	A1	A0
A0	0	0	0
A2	0	0	1
A4	0	1	0
A6	0	1	1
A8	1	0	0
AA	1	0	1
AC	1	1	0
AE	1	1	1

PIN DESCRIPTION



Top View



Top View

Ball Pitch 0.4mm*0.5mm Package Type Z = A				Ball Pitch 0.4mm*0.4mm Package Type Z = B
Pin #		**Symbol**	**Type**	**Function**
0.4mm*0.5mm	**0.4mm*0.4mm**			
4	4	SDA	I/O	Serial Data
2	3	SCL	I	Serial Clock Input
3	2	GND	P	Ground
1	1	V_{CC}	P	Power Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3V ~ +6.5V
Input / Output Voltage	GND-0.3V ~ V_{CC}+0.3V
Operating Ambient Temperature	-40°C ~ +85°C
Storage Temperature	-65°C ~ +150°C

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CAPACITANCE

Applicable over recommended operating range from: T_A = 25℃, f = 1.0MHz, V_{CC} = +1.7V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input / Output Capacitance(SDA)	$C_{I/O}$	V_{IO}=0V	-	-	8	pF
Input Capacitance(A0,A1,A2,SCL)	C_{IN}	V_{IN}=0V	-	-	6	pF

DC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +3.6V, unless otherwise noted

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC1}		1.7	-	3.6	V
Supply Current V_{CC}=1.8V	I_{CC1}	READ at 400kHZ	-	0.14	0.3	mA
Supply Current V_{CC}=1.8V	I_{CC2}	WRITE at 400kHZ	-	0.28	0.5	mA
Supply Current V_{CC}=1.8V	I_{SB1}	V_{IN} = V_{CC} or V_{SS}	-	0.03	0.5	μA
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or V_{SS}	-	0.10	1.0	μA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} or V_{SS}	-	0.05	1.0	μA
Input Low Level	V_{IL1}	V_{CC} = 1.7V to 5.5V	-0.3	-	V_{CC}x0.3	V
Input High Level	V_{IH1}	V_{CC} = 1.7V to 5.5V	V_{CC}x0.7	-	V_{CC}+0.3	V
Output Low Level V_{CC} = 1.7V	V_{OL1}	I_{OL} = 0.15mA	-	-	0.2	V
Output Low Level V_{CC} = 5.0V	V_{OL2}	I_{OL} = 3.0mA	-	-	0.4	V

AC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +3.6V, C_L = 1 TTL Gate and 100pF, unless otherwise noted

Parameter	Symbol	400 kHz			1 MHz			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency, SCL	f_{SCL}	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	t_{LOW}	1.3	-	-	0.5	-	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	-	0.26	-	-	μs
Noise Suppression Time	t_I	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t_{AA}	-	-	0.9	-	-	0.45	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.3	-	-	0.5	-	-	μs
Start Hold Time	$t_{HD.STA}$	0.6	-	-	0.25	-	-	μs
Start Setup Time	$t_{SU.STA}$	0.6	-	-	0.25	-	-	μs
Data In Hold Time	$t_{HD.DAT}$	0	-	-	0	-	-	μs
Data In Setup Time	$t_{SU.DAT}$	100	-	-	100	-	-	ns
Input Rise Time[NOTE1]	t_R	-	-	0.3	-	-	0.12	μs
Input Fall Time[NOTE1]	t_F	-	-	0.3	-	-	0.12	μs
Stop Setup Time	$t_{SU.STO}$	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	t_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	1.9	3	-	1.9	3	ms
5.0V, 25℃, Byte Mode[NOTE1]	Endurance	1M	-	-	1M	-	-	Write Cycles

NOTE1: This parameter is characterized and is not 100% tested.

NOTE2: AC measurement conditions: R_L(connects to V_{CC}): 1.3k

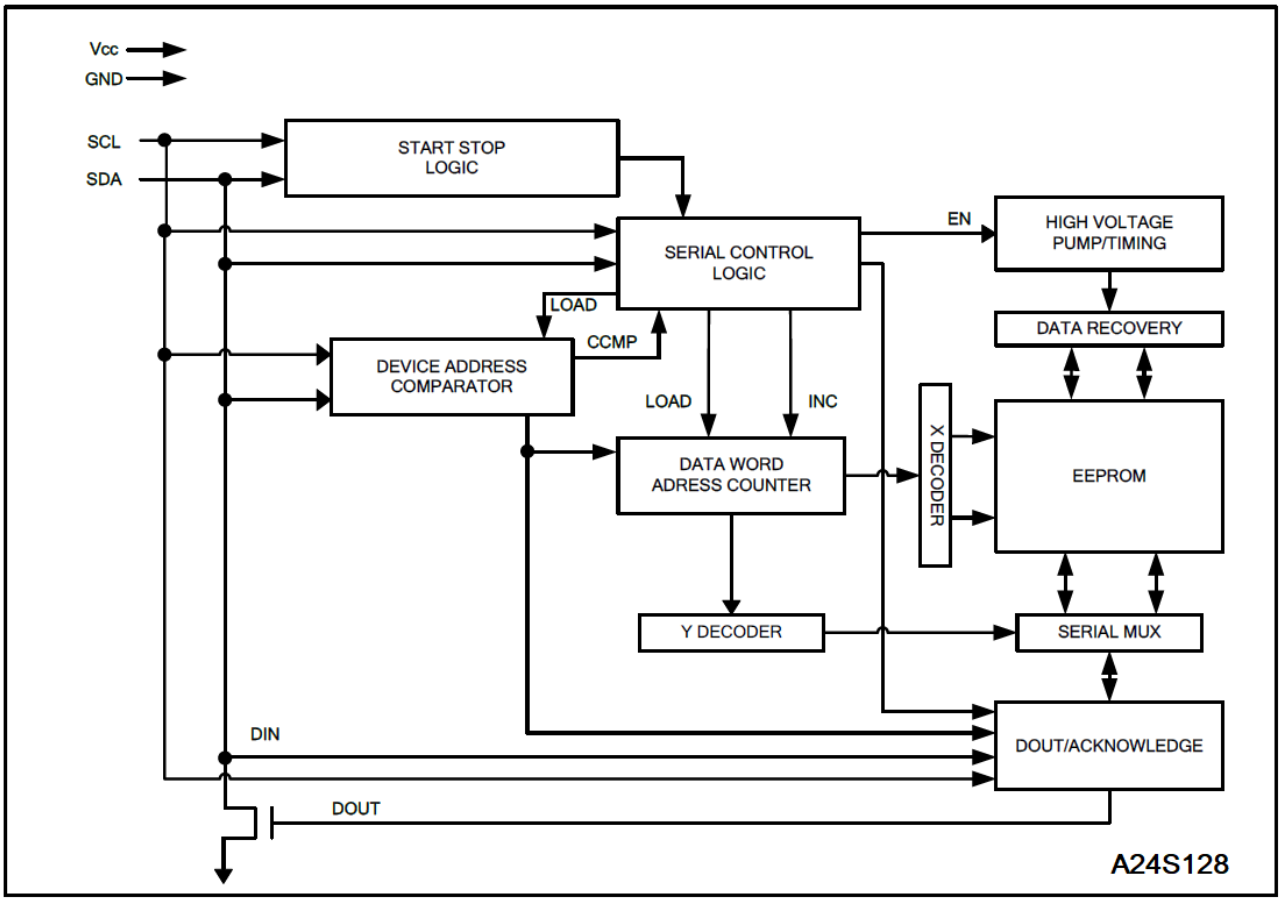
Input pulse voltages: 0.3V_{CC} to 0.7V_{CC}

Input rise and fall time: 50ns

Input and output timing reference voltages: 0.5V_{CC}

The value of R_L should be concerned according to the actual loading on the user's system.

BLOCK DIAGRAM



DETAILED INFORMATION

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

FUNCTIONAL DESCRIPTION

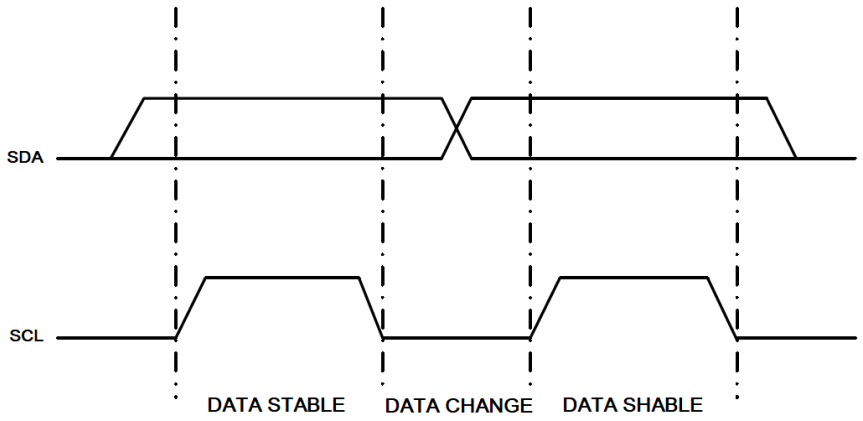
1. Memory Organization

A24S128, 128k SERIAL EEPROM: Internally organized with 256 pages of 64 bytes each, the 128k requires a 14-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

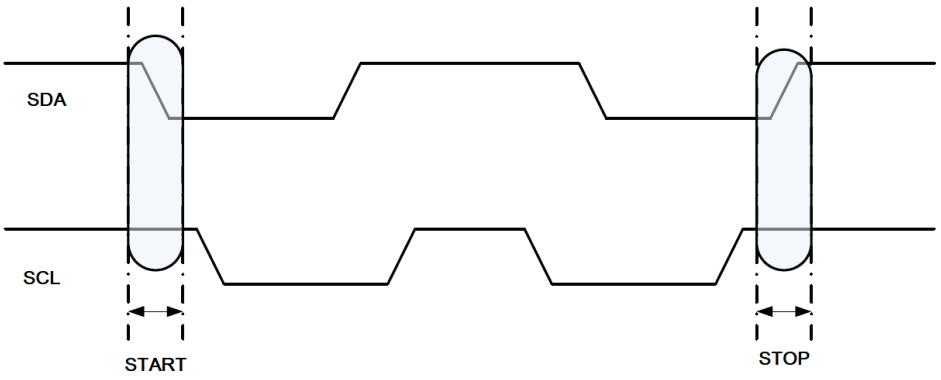
Figure1. Data Validity



START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2).

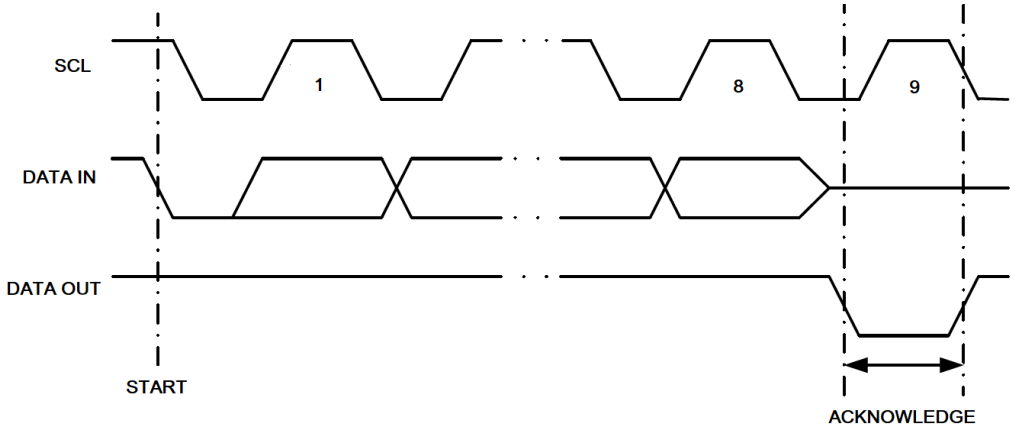
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 2).

Figure 2. Start and Stop Definition



ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 3. Output Acknowledge



STANDBY MODE: The A24S128 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Lock SDA high in each cycle while SCL is high.
3. Create a start condition.

3. Device Addressing

The 128k EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4)

Figure 4. Device Address

MSB							LSB
1	0	1	0	A2	A1	A0	R/W

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The fifth, sixth and seventh bits of the device address can be configured，default to 000b.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

A24S128 consists of a series of products with different fab-out default device address.

Table 1

Part Number	A2	A1	A0
A24S128-A0	0	0	0
A24S128-A2	0	0	1
A24S128-A4	0	1	0
A24S128-A6	0	1	1
A24S128-A8	1	0	0
A24S128-AA	1	0	1
A24S128-AC	1	1	0
A24S128-AE	1	1	1

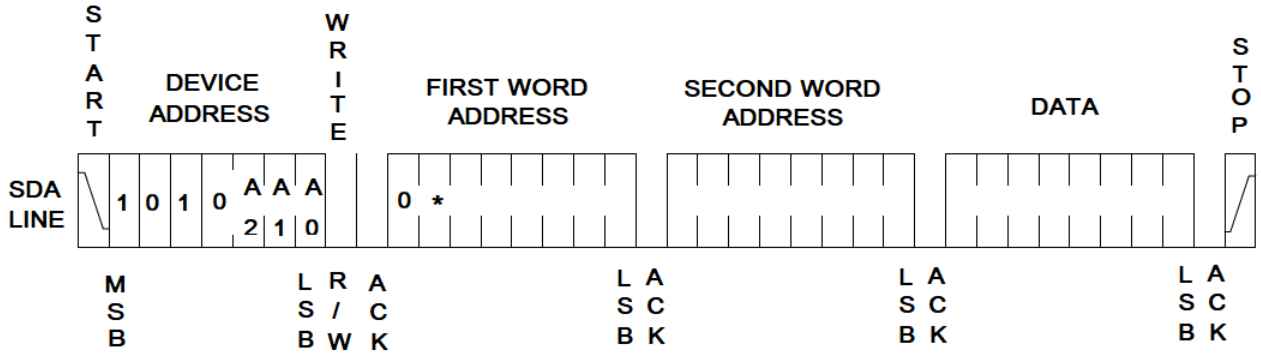
4. Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address, as as Figure 5, following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 6).

Figure 5. Date Word Address

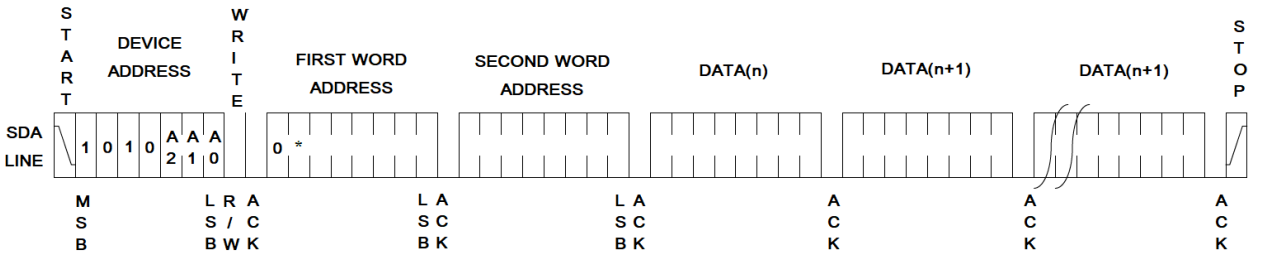
0	*	B13	B12	B11	B10	B9	B8
B7	B6	B5	B4	B3	B2	B1	B0

Figure 6. Byte Write



PAGE WRITE: The 128K EEPROM is capable of a 64-byte page writes. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 7).

Figure 7. Page Write



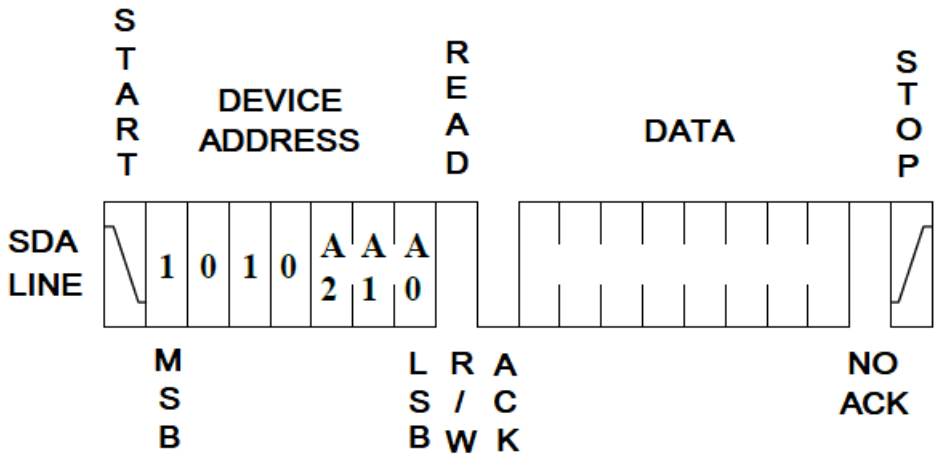
The data word address lower six bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

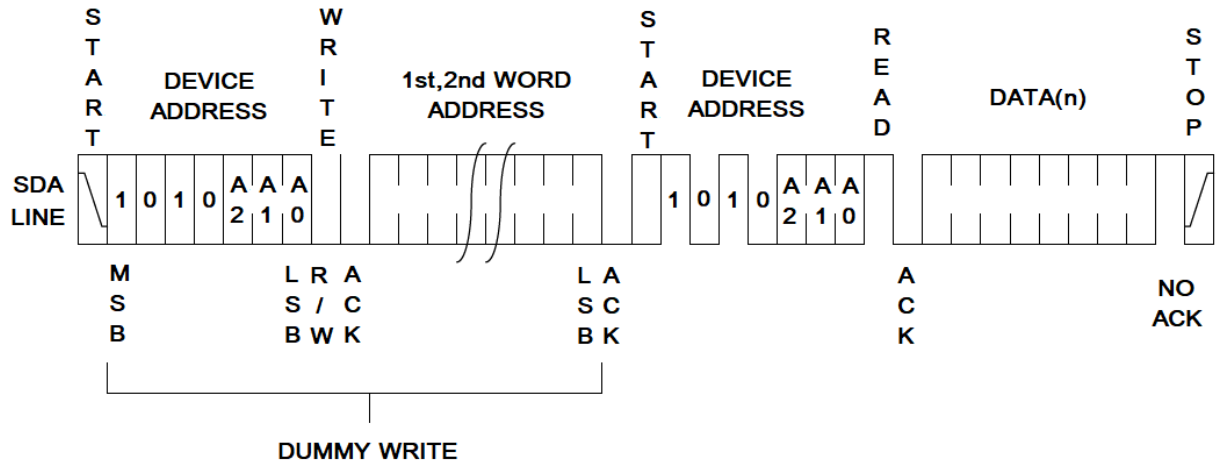
CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 8).

Figure 8. Current Address Read



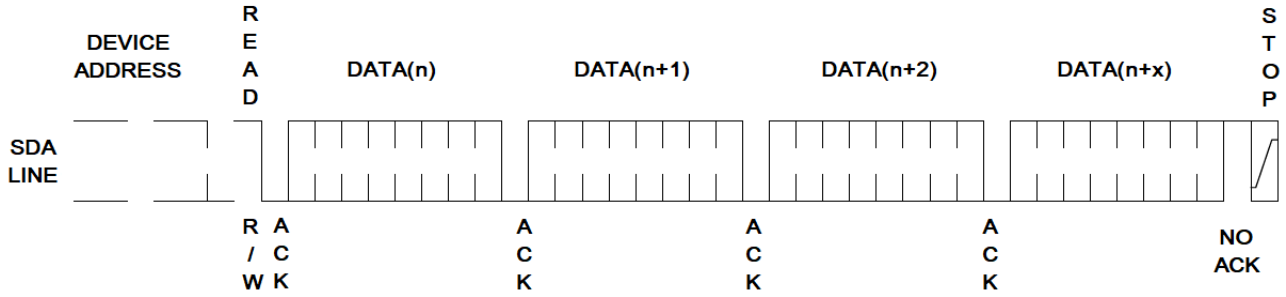
RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9)

Figure 9. Random Read



SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 10).

Figure 10. Sequential Read



6. Software write protection configuration

By writing specific values in a register (Table 2) located at address 11xx.xxxx.xxxx.xxxxb, the memory array can be write-protected by blocks.

Table 2

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write	★	★	★	★	Partial Write protect activation	Size of write protected block	Size of write protected block	★
Read	0	0	0	0				0

NOTE:

Bit 7 – 4 and bit 0 are don't care bits.

Bit 3 enables or disables the partial write protection.

Bit 3=0: the whole memory can be written (no write protection)

Bit 3=1: the concerned block is write-protected

Bits 2 and 1 define the size of the memory block to be protected against write instructions:

Bit 2, Bit 1= 0, 0: the upper quarter of memory is write-protected

Bit 2, Bit 1= 0, 1: the upper half memory is write-protected

Bit 2, Bit 1= 1, 0: the upper 3/4 of memory are write-protected

Bit 2, Bit 1= 1, 1: the whole memory is write-protected

The device is delivered with the Write Protect register set to 0 (00h).

7. Device Addressing configuration

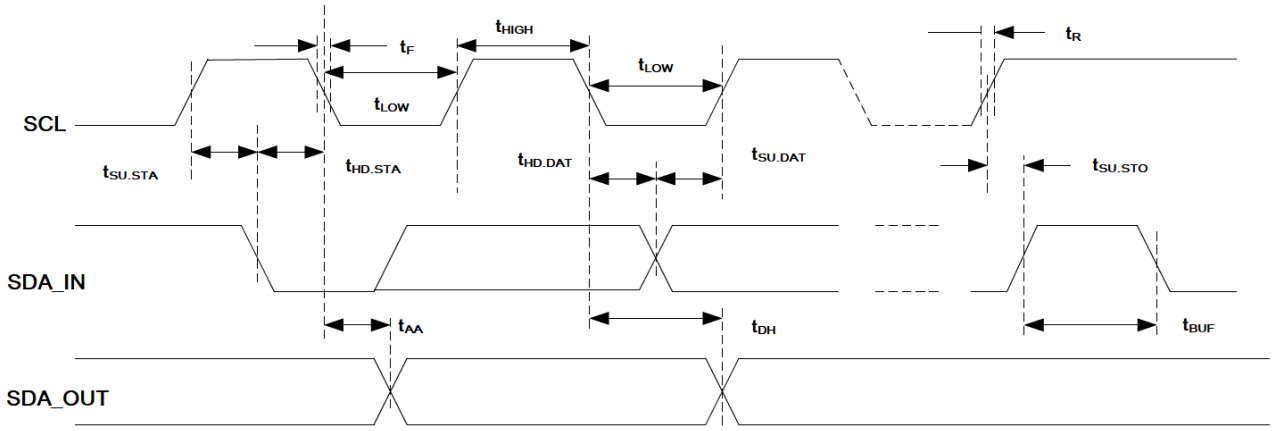
By writing specific values in a register (Table 3) located at address 10xx.xxxx.xxxx.xxxxb, the device address can be reconfigured.

Table 3

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write	★	★	★	★	★	A2	A1	A0
Read	0	0	0	0	0			

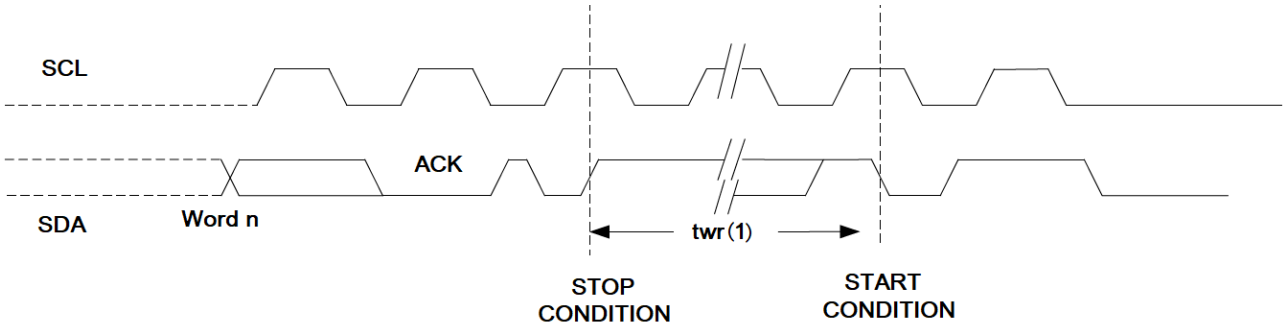
Bus Timing

Figure 11. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

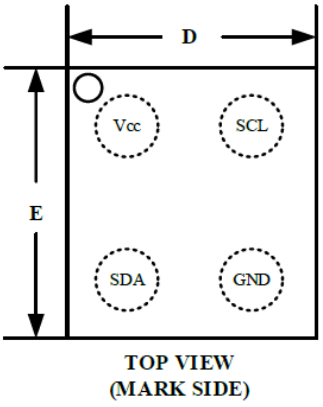
Figure 12. SCL: Serial Clock, SDA: Serial Data I/O



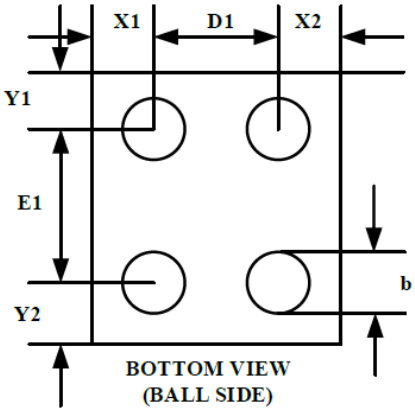
NOTE: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

PACKAGE INFORMATION

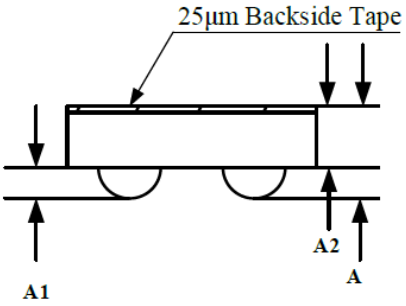
Dimension in CSP4 Ball Pitch 0.4mm*0.5mm (Unit: mm)



TOP VIEW
(MARK SIDE)



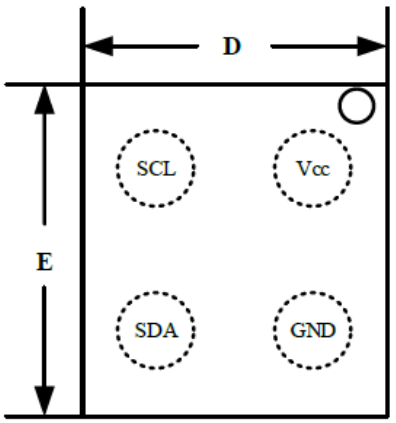
BOTTOM VIEW
(BALL SIDE)



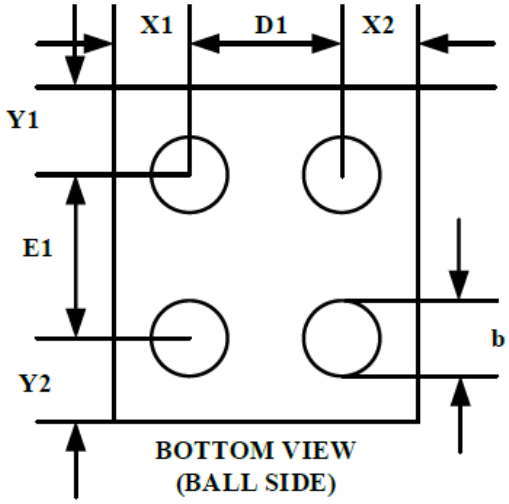
SIDE VIEW

Symbol	Min	Max
A	0.250	0.310
A1	0.045	0.065
A2	0.205	0.245
D	0.637	0.687
D1	0.400BSC	
E	0.726	0.776
E1	0.500BSC	
b	0.140	0.180
x1	0.131REF	
x2	0.131REF	
y1	0.126REF	
y2	0.126REF	

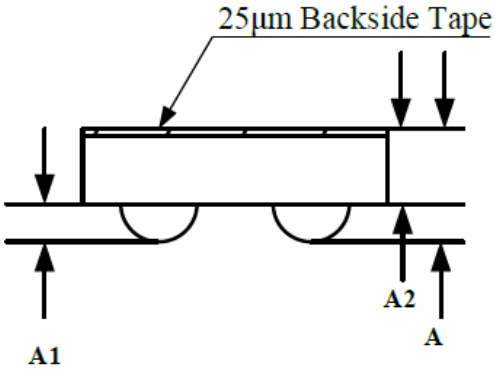
Dimension in CSP4 Ball Pitch 0.4mm*0.4mm (Unit: mm)



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

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A2	0.205	0.245
D	0.637	0.687
D1	0.400BSC	
E	0.726	0.776
E1	0.40BSC	
b	0.140	0.180
x1	0.131REF	
x2	0.131REF	
y1	0.176REF	
y2	0.176REF	

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