## DESCRIPTION

The A4809C is a cost-effective system supervisor Integrated Circuit (IC) designed to monitor $V_{CC}$ in digital and mixed signal systems and provide a warning signal when the system power supply is out of working range, and a reset signal to the host processor when necessary. No external components are required.

It features low supply current. Both CMOS and N-channel open drain output configurations are available. Since the delay circuit is built-in, peripherals are unnecessary and high density mounting is possible.

A4809C is available in SOT-23 package.

## ORDERING INFORMATION

| Package Type | Part Number | |
|---|---|---|
| SOT-23 | E3 | A4809CE3R-XXXDZ |
| | | A4809CE3VR-XXXDZ |
| Note | XXX: Detector Voltage<br>263=2.63V 293=2.93V<br>308=3.08V<br>D: Delay Time<br>50ms~200ms<br>Z: C=CMOS, N=Nch<br>V: Halogen Free Package<br>R: Tape & Reel | |
| AiT provides all RoHS products<br>Suffix "V" means Halogen free Package | | |

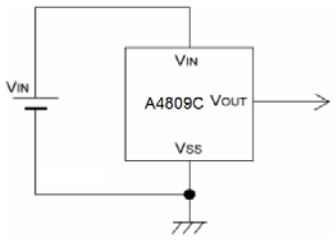
## FEATURES

- Precision $V_{CC}$ Monitor for 2.63V, 2.93V, 3.08V
- Highly Accurate: ± 1%
- Low Power Consumption : lower than 1.5μA
- Operating Voltage Range: 0.7V ~ 6.0V
- Detect Voltage Temperature Characteristics: ±100ppm/℃(TYP.)
- Built-In Delay Circuit: 50ms ~ 200ms
- Output Configuration: N-channel open drain or CMOS
- Available in SOT-23 package

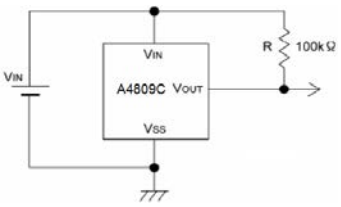
## APPLICATION

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors
- Delay circuitry

## TYPICAL APPLICATION

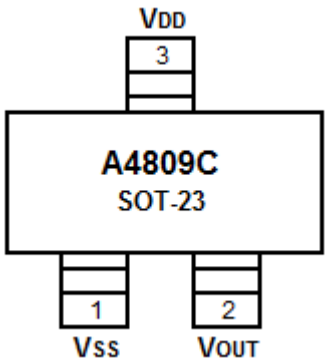



CMOS output




N-channel open drain output

## PIN DESCRIPTION




Top View

| Pin # | Symbol | Function |
|---|---|---|
| 1 | $V_{SS}$ | GND Pin |
| 2 | $V_{OUT}$ | Output Voltage |
| 3 | $V_{DD}$ | Input Voltage |

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| $V_{IN}$, Input Supply Voltage | | 6V |
| $I_{OUT}$, Output Current | | 30mA |
| $V_{OUT}$, Output Voltage | CMOS | $V_{SS}$-0.3V~ $V_{IN}$ +0.3V |
| | N-ch open drain | $V_{SS}$-0.3V~6V |
| $P_D$, Power Dissipation | SOT-23 | 150mW |
| $T_{OPR}$, Operating Temperature Range | | -30 °C ~+85°C |
| $T_{STG}$, Storage Temperature Range | | -40 °C ~+125°C |

Stresses beyond may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Detect Voltage | $V_{DF}$ | | | $V_{DF}(T)$ ×0.98 | $V_{DF}(T)$ | $V_{DF}(T)$ ×1.02 | V |
| Hysteresis Range | $V_{HYS}$ | | | $V_{DF}$ ×0.002 | $V_{DF}$ ×0.005 | $V_{DF}$ ×0.008 | V |
| Supply Current | $I_{SS}$ | $V_{IN}$=1.5V | | | 1.0 | 1.2 | uA |
| | | $V_{IN}$=2.0V | | | 1.0 | 1.3 | |
| | | $V_{IN}$=3.0V | | | 1.1 | 1.3 | |
| | | $V_{IN}$=4.0V | | | 1.1 | 1.3 | |
| | | $V_{IN}$=5.0V | | | 1.2 | 1.5 | |
| Operating Voltage | $V_{IN}$ | $V_{DF}$= 2.63V to 3.08V | | 0.7 | | 6 | V |
| Output Current | $I_{OUT}$ | N-ch $V_{DF}$=0.5V | $V_{IN}$=1.5V | | 2 | | mA |
| | | | $V_{IN}$=2.0V | | 7 | | |
| | | | $V_{IN}$=3.0V | | 10 | | |
| | | | $V_{IN}$=4.0V | | 11 | | |
| | | | $V_{IN}$=5.0V | | 13 | | |
| | | CMOS, P-ch $V_{DF}$=2.63V $V_{IN}$=6.0V | | | -10 | | |
| Detect Voltage Temperature Characteristics | $\Delta V_{DF}$ $\Delta T_{OPR} \times V_{DF}$ | | | | ±100 | | ppm/°C |
| Transient Delay time ($V_{DR} \rightarrow V_{OUT}$ inversion) | $T_{DLY}$* | $V_{IN}$ changes from 0.7V to 6V | | 50 | | 200 | ms |

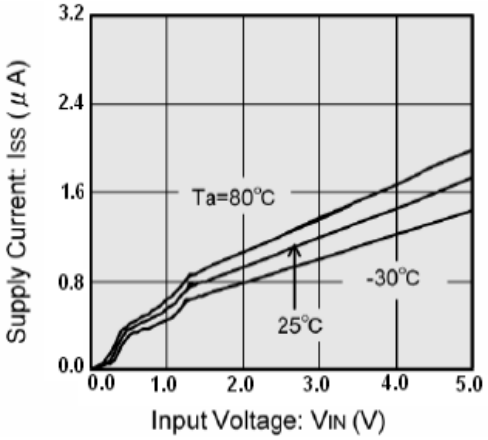
NOTE1: $V_{DF}(T)$: Setting detect voltage value

NOTE2: Release Voltage: $V_{DR} = V_{DF} + V_{HYS}$

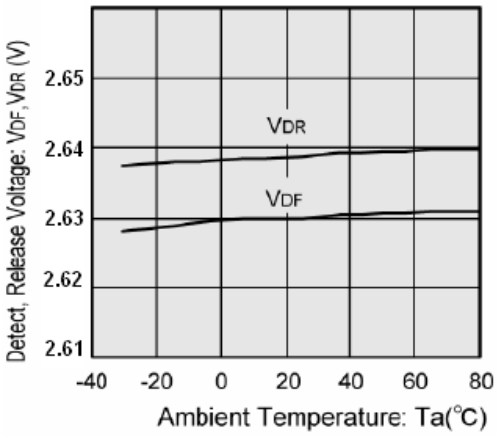
NOTE3: The power consumption during power-start to output being stable (release operation) is 2μA greater than it is after that period (completion of release operation) because of delay circuit through current.

## TYPICAL PERFORMANCE CHARACTERISTIC

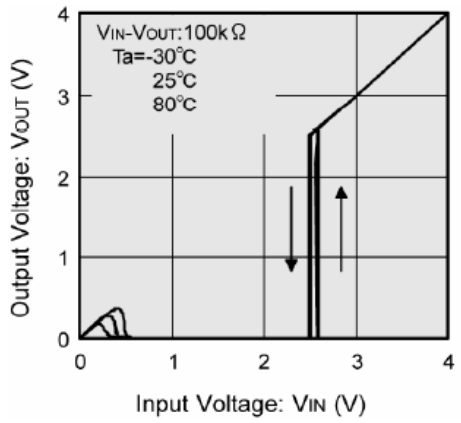
1. Supply Current vs. Input Voltage



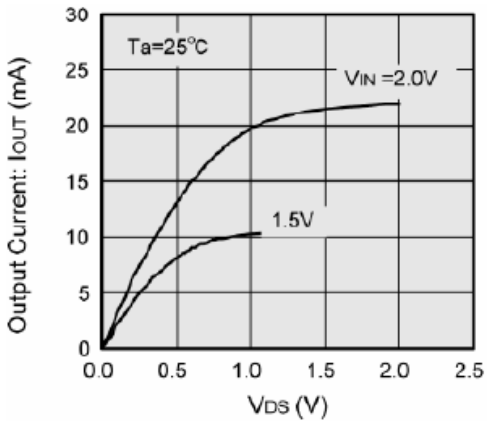

2. Detect Voltage, Release Voltage vs. Ambient Temperature



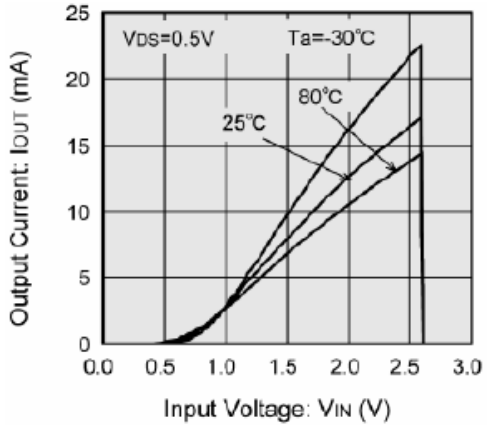

3. Output Voltage vs. Input Voltage



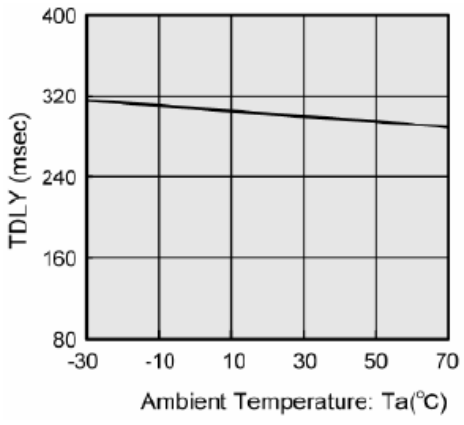

4. N-Channel Driver Output Current vs. $V_{DS}$



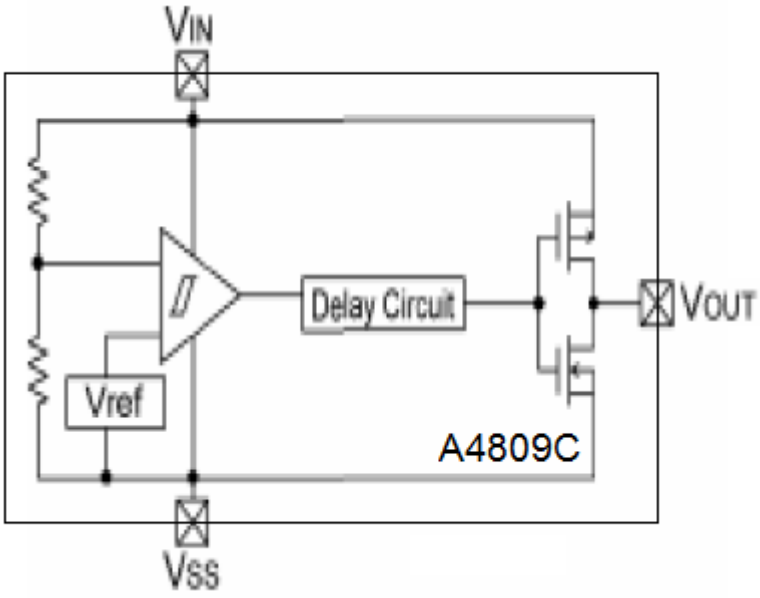

5. N-Channel Driver Output Current vs. Input Voltage



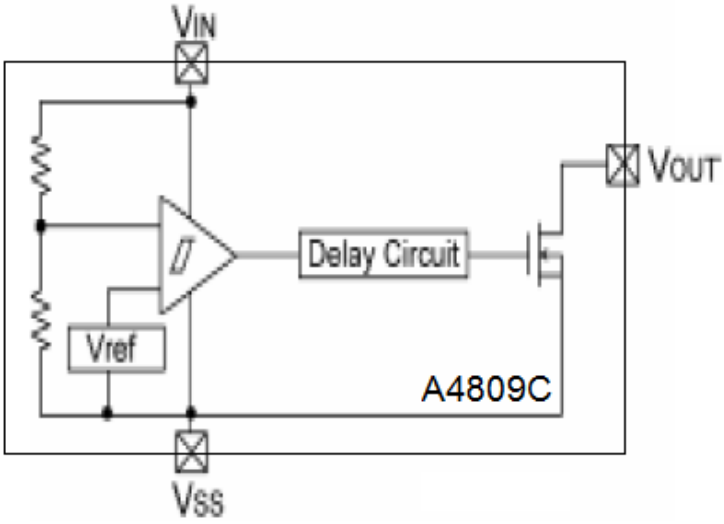

6. Ambient Temperature vs. Transient Delay Time



## BLOCK DIAGRAM




CMOS output




N-channel open drain output

## DETAILED INFORMATION

### Operational Explanation

**CMOS output (the 4th is the most important)**

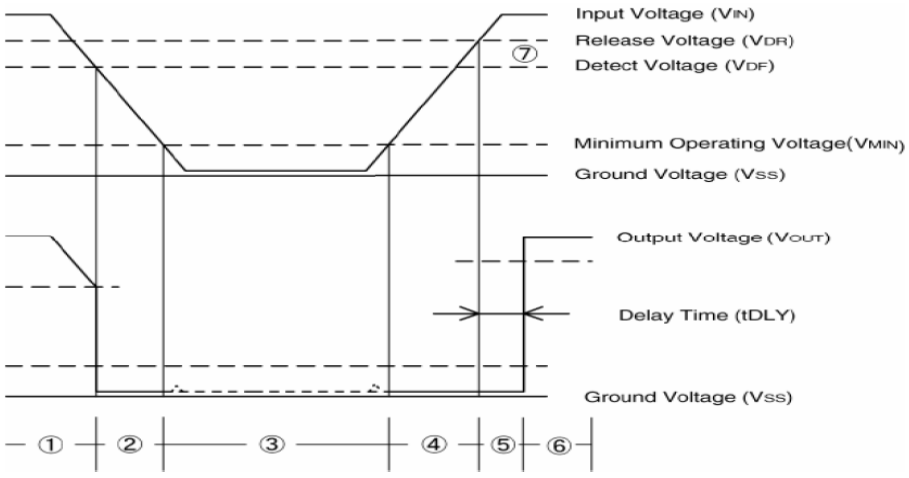
1. When a voltage higher than the release voltage ($V_{DR}$) is applied to the voltage input pin ($V_{IN}$), the voltage will gradually fall. When a voltage higher than the detect voltage ($V_{DF}$) is applied to $V_{IN}$, output ($V_{OUT}$) will be equal to the input at $V_{IN}$. Note that high impedance exists at $V_{OUT}$ with the N-channel open drain configuration. If the pin is pulled up, $V_{OUT}$ will be equal to the pull up voltage.
2. When $V_{IN}$ falls below $V_{DF}$, $V_{OUT}$ will be equal to the ground voltage ($V_{SS}$) level (detect state). Note that this also applies to N-channel open drain configurations.
3. When $V_{IN}$ falls to a level below that of the minimum operating voltage ($V_{MIN}$ ) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.
4. When $V_{IN}$ rises above the $V_{SS}$ level (excepting levels lower than minimum operating voltage), $V_{OUT}$ will be equal to $V_{SS}$ until $V_{IN}$ reaches the $V_{DR}$ level. But if the rising rate is fast enough, $V_{OUT}$ is equal to the pull up voltage.
5. Although $V_{IN}$ will rise to a level higher than $V_{DR}$, $V_{OUT}$ maintains ground voltage level via the delay circuit.
6. Following transient delay time, $V_{IN}$ will be output at $V_{OUT}$.

Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

Notes:

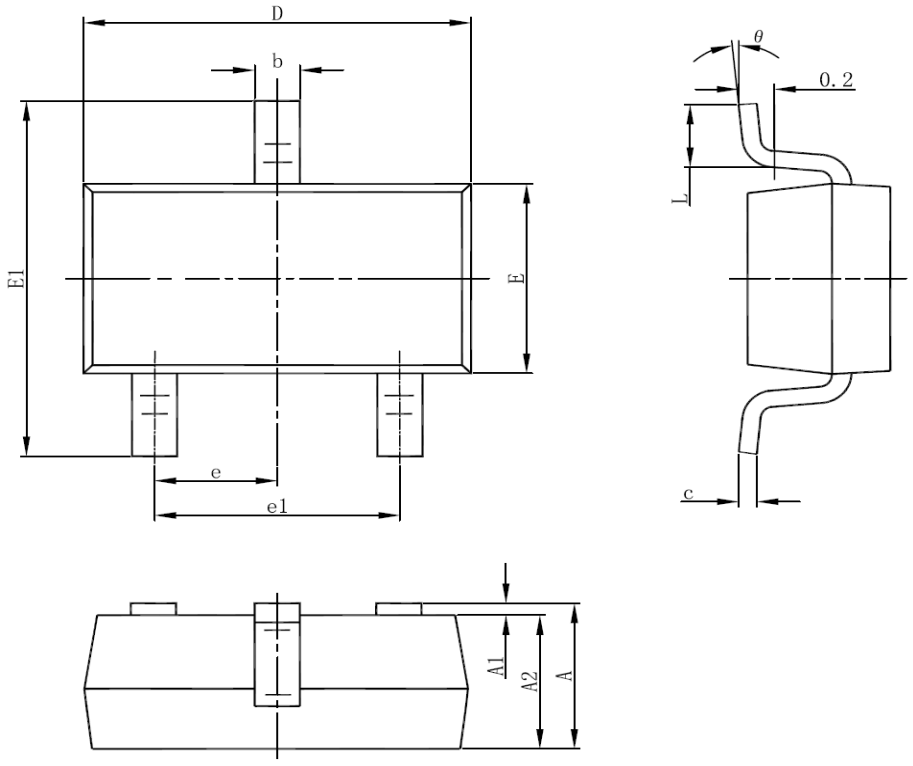
1. The difference between $V_{DR}$ and $V_{DF}$ represents the hysteresis range.
2. Propagation delay time ($t_{DLY}$) represents the time it takes for $V_{IN}$ to appear at $V_{OUT}$ once the said voltage has exceeded the $V_{DR}$ level.

Timing Chart



## PACKAGE INFORMATION

Dimension in SOT-23 Package (Unit: mm)




| Symbol | Min | Max |
|---|---|---|
| A | 1.050 | 1.250 |
| A1 | 0.000 | 0.100 |
| A2 | 1.050 | 1.150 |
| b | 0.300 | 0.500 |
| c | 0.100 | 0.200 |
| D | 2.820 | 3.020 |
| E | 1.500 | 1.700 |
| E1 | 2.650 | 2.950 |
| e | 0.950(BSC) | |
| e1 | 1.800 | 2.000 |
| L | 0.300 | 0.600 |
| θ | 0° | 8° |

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