DESCRIPTION

The A4808 is a micro-power voltage detector supervising the power supply voltage level for microprocessors or digital systems, which is extremely accurate with minimal temperature drift.
It provides internally fixed threshold levels with 0.1V per step ranging from 1.5V to 5V, which covers most digital applications. It features low supply current. Both CMOS and N-channel open drain output configurations are available. Since the delay circuit is built-in, peripherals are unnecessary and high density mounting is possible.

The A4808 is available in SOT-23 package.

ORDERING INFORMATION

Package Type	Part Number	
SOT-23	E3	A4808E3R-XXDI
		A4808E3VR-XXDI
Note	XX: Detect Voltage 15=1.5V, 30=3.0V D: Delay time: 50ms~200ms I: N: Nch, C: CMOS V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products Suffix " V " means Halogen free Package		

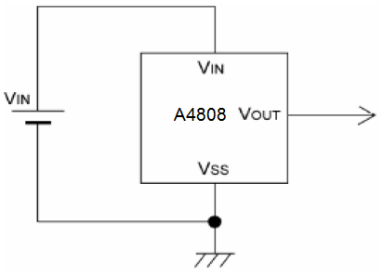
FEATURES

- Highly Accurate: ± 2%
- Low Power Consumption : lower than 1.5μA
- Detect Voltage Range: 1.5V ~ 5.0V in 0.1V increments
- Operating Voltage Range: 0.7V ~ 7.0V
- Detect Voltage Temperature Characteristics: ±100ppm/°C(TYP.)
- Built-In Delay Circuit: 1ms ~ 50ms
  50ms ~ 200ms
  80ms ~ 400ms
- Output Configuration:
  N-channel open drain or CMOS
- Available in SOT-23 Package

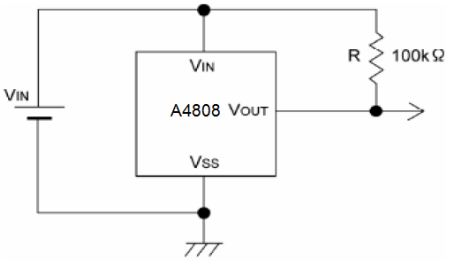
APPLICATION

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors
- Delay circuitry

TYPICAL APPLICATION

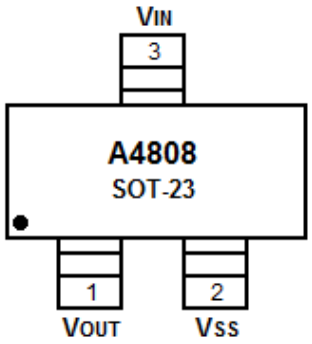


COMS output



N-channel open drain output

PIN DESCRIPTION



Top View

Pin #	Symbol	Function
1	V_{OUT}	Output
2	V_{SS}	Ground
3	V_{IN}	Supply Voltage Input

ABSOLUTE MAXIMUM RATINGS

V_{IN}, Input Supply Voltage		12V
I_{OUT}, Output Current		30mA
V_{OUT}, Output Voltage	CMOS	V_{SS}-0.3V~ V_{IN} +0.3V
	N-ch open drain	V_{SS}-0.3V~9V
P_D, Power Dissipation	SOT-23	150mW
T_{OPR}, Operating Temperature Range		-30°C ~+85°C
T_{STG}, Storage Temperature Range		-40°C ~+125°C

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A=25°C

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Detect Voltage	V_{DF}			$V_{DF}(T)$ ×0.98	$V_{DF}(T)$	$V_{DF}(T)$ ×1.02	V
Hysteresis Range	V_{HYS}			V_{DF} ×0.02	V_{DF} ×0.05	V_{DF} ×0.08	V
Supply Current	I_{SS}	V_{IN}=1.5V			1.2	2.0	uA
		V_{IN}=2.0V			1.3	2.5	
		V_{IN}=3.0V			1.3	3.0	
		V_{IN}=4.0V			1.4	3.5	
		V_{IN}=5.0V			1.6	4	
Operating Voltage	V_{IN}	V_{DF}= 1.6V to 6.0V		0.7		7	V
Output Current	I_{OUT}	N-ch V_{DF}=0.5V	V_{IN}=1.5V		2		mA
			V_{IN}=2.0V		7		
			V_{IN}=3.0V		10		
			V_{IN}=4.0V		11		
			V_{IN}=5.0V		13		
		CMOS, P-ch V_{DF}=2.1V V_{IN}=8.0V			-10		
Detect Voltage Temperature Characteristics	$\frac{\Delta V_{DF}}{\Delta T_{OPR} \times V_{DF}}$				±100		ppm/°C
Transient Delay time (V_{DR} → V_{OUT} inversion)	T_{DLY}*	V_{IN} changes from 0.7V to 7V		20		200	ms

NOTE1: $V_{DF}(T)$: Setting detect voltage value

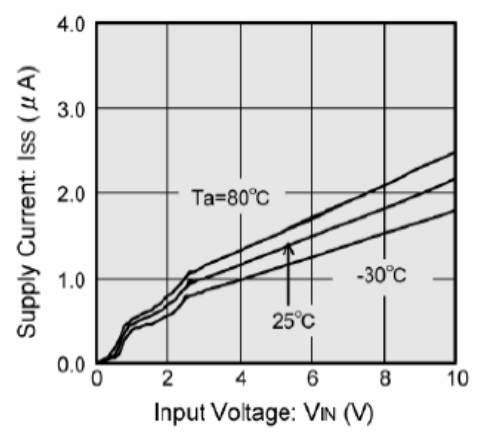
NOTE2: Release Voltage: $V_{DR} = V_{DF} + V_{HYS}$

NOTE3: * Transient Delay Time: 1ms to 50ms & 80ms to 400ms versions are also available.

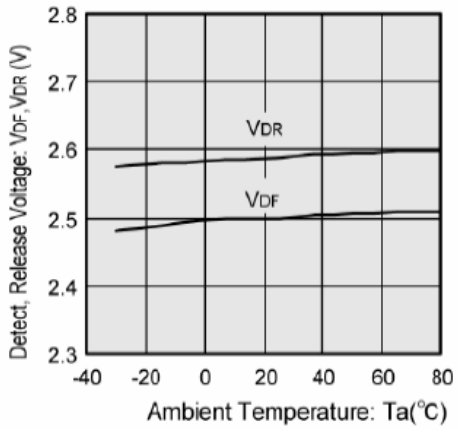
NOTE4: The power consumption during power-start to output being stable (release operation) is 2μA greater than it is after that period (completion of release operation) because of delay circuit through current.

TYPICAL PERFORMANCE CHARACTERISTICS

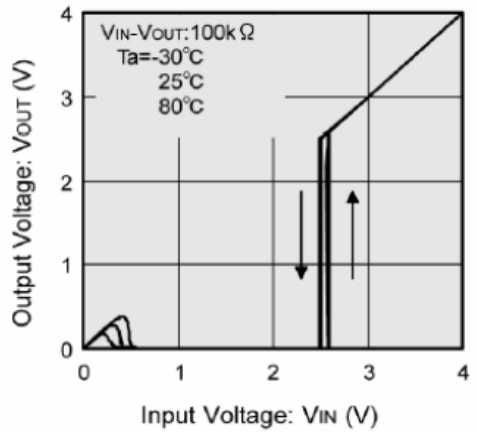
1. Supply Current vs. Input Voltage



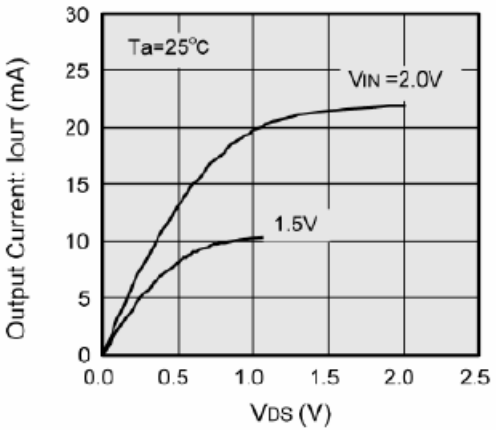
2. Detect Voltage, Release Voltage vs. Ambient Temperature



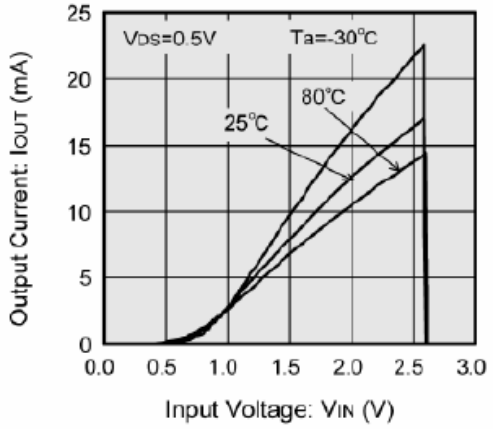
3. Output Voltage vs. Input Voltage



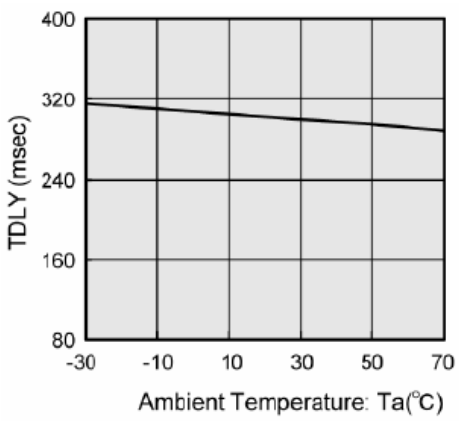
4. N-Channel Driver Output Current vs. VDS



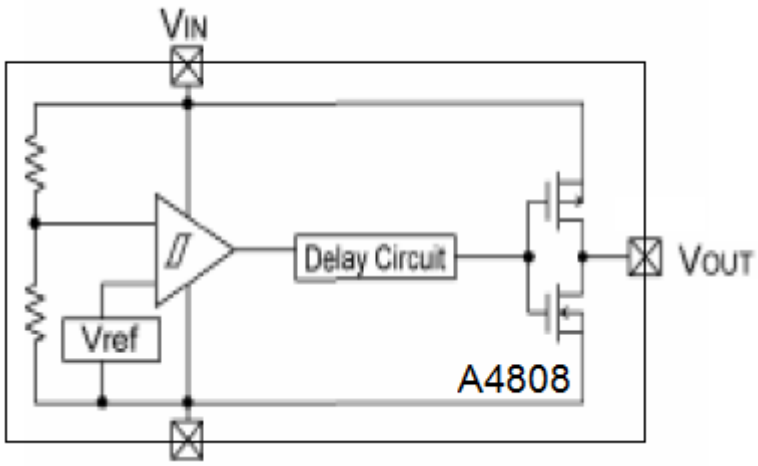
5. N-Channel Driver Output Current vs. Input Voltage



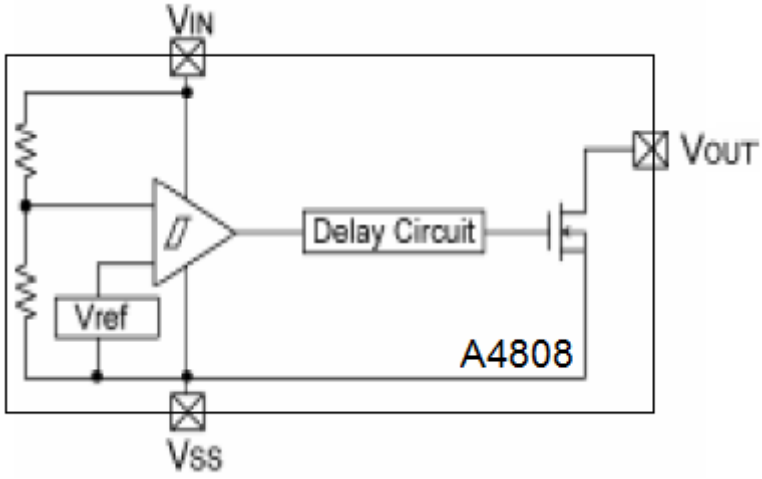
6. Ambient Temperature vs. Transient Delay Time



BLOCK DIAGRAM



COMS output



N-channel open drain output

DETAILED INFORMATION

Operational Explanation

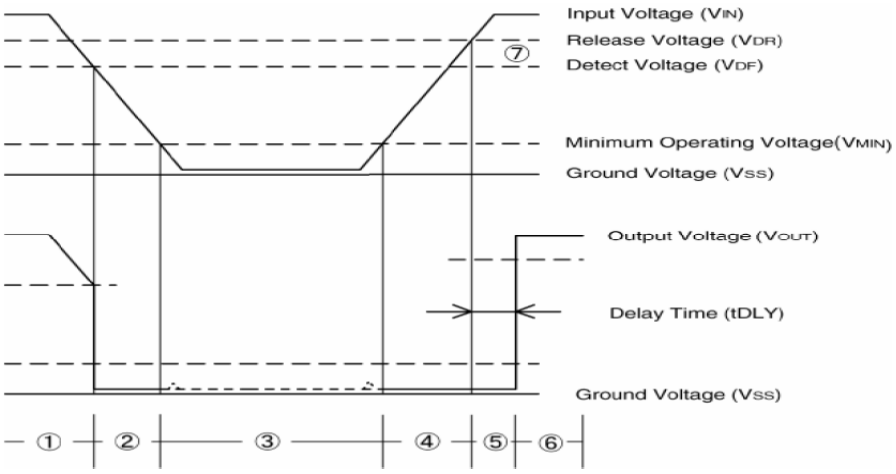
CMOS output (the 4th is the most important)

1. When a voltage higher than the release voltage (V_{DR}) is applied to the voltage input pin (V_{IN}), the voltage will gradually fall. When a voltage higher than the detect voltage (V_{DF}) is applied to V_{IN}, output (V_{OUT}) will be equal to the input at V_{IN}. Note that high impedance exists at V_{OUT} with the N-channel open drain configuration. If the pin is pulled up, V_{OUT} will be equal to the pull up voltage.
2. When V_{IN} falls below V_{DF}, V_{OUT} will be equal to the ground voltage (V_{SS}) level (detect state). Note that this also applies to N-channel open drain configurations.
3. When V_{IN} falls to a level below that of the minimum operating voltage (V_{MIN}) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.
4. When V_{IN} rises above the V_{SS} level (excepting levels lower than minimum operating voltage), V_{OUT} will be equal to V_{SS} until V_{IN} reaches the V_{DR} level. But if the rising rate is fast enough, V_{OUT} is equal to the pull up voltage.
5. Although V_{IN} will rise to a level higher than V_{DR}, V_{OUT} maintains ground voltage level via the delay circuit.
6. Following transient delay time, V_{IN} will be output at V_{OUT}. Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

Notes:

1. The difference between V_{DR} and V_{DF} represents the hysteresis range.
2. Propagation delay time (t_{DLY}) represents the time it takes for V_{IN} to appear at V_{OUT} once the said voltage has exceeded the V_{DR} level.

Timing Chart



Directions for Use

Notes on Use

1. Please use this IC within the stated maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at R_{IN} if load current (I_{OUT}) exists. It is therefore recommend that no resistor be added. (refer to Oscillation Description (1) below)
3. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (I_{OUT}) does not exist. (refer to Oscillation Description (2) below)
4. With a resistor connected between the V_{IN} pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{IN} pin.
5. If a resistor (R_{IN}) must be used, then please use with as small a level of input impedance as possible in order to control the occurrences of oscillation as described above.

   Further, please ensure that R_{IN} is less than 10kΩ and that C_{IN} is more than 0.1μF (Figure 1). In such cases, detect and release voltages will rise due to voltage drops at R_{IN} brought about by the IC's supply current.

Oscillation Description

(1) Oscillation as a result of output current with the CMOS output configuration:

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (I_{OUT}) will flow through RL. Because a voltage drop (R_{IN} x I_{OUT}) is produced at the R_{IN} resistor, located between the input (IN) and the V_{IN} pin, the load current will flow via the IC's V_{IN} pin. The voltage drop will also lead to a fall in the voltage level at the V_{IN} pin. When the V_{IN} pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at R_{IN} will disappear, the voltage level at the V_{IN} pin will rise and release operations will begin over again.

Oscillation may occur with this " release - detect - release " repetition.

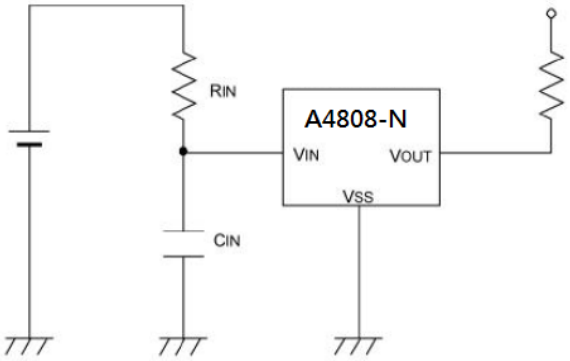
Further, this condition will also appear via means of a similar mechanism during detect operations.

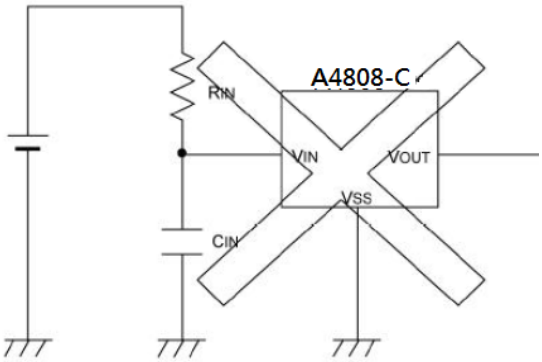
(2) Oscillation as a result of through current:

Since the series are CMOS ICS, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur during release voltage operations as a result of output current which is influenced by this through current (Figure 3).

Since hysteresis exists during detect operations, oscillation is unlikely to occur.

Figure 1. When using an input resistor





Oscillation Description

Figure 2.Oscillation in relation to output current

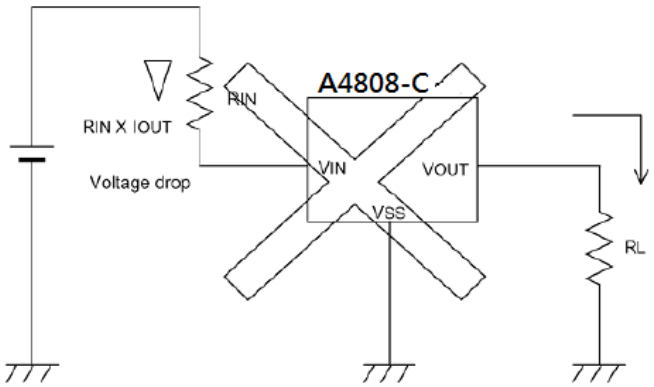
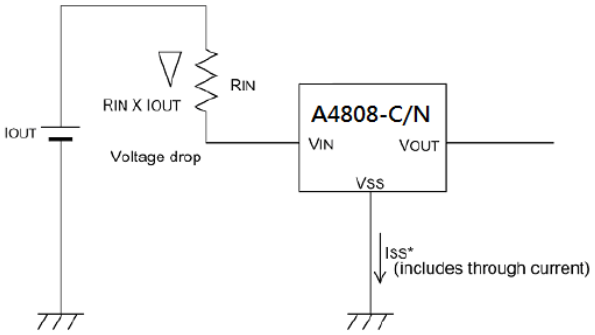
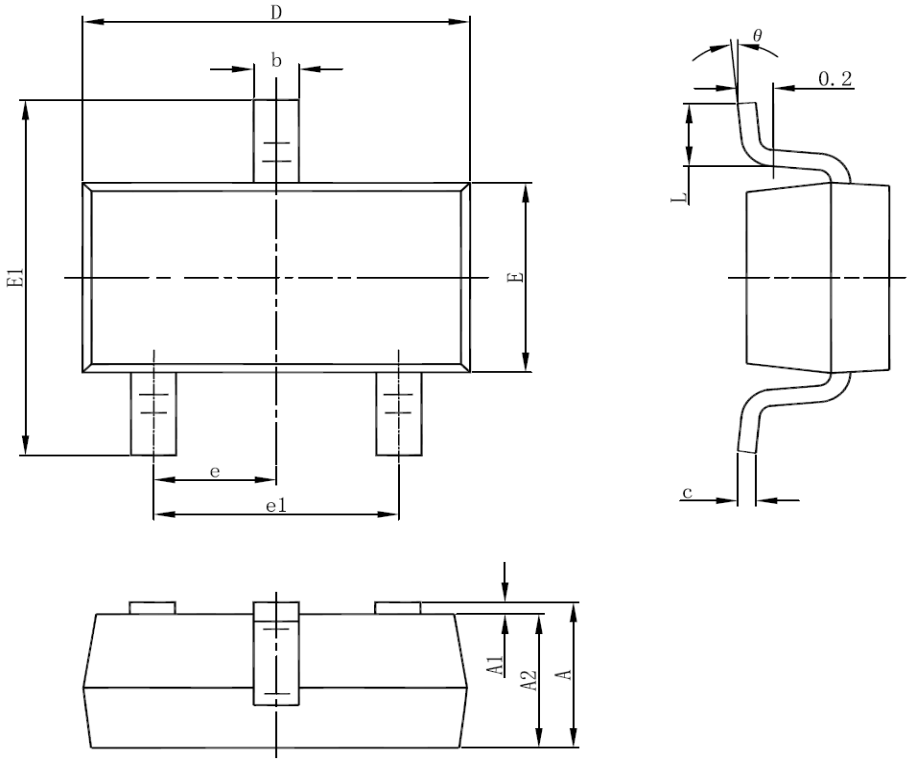


Figure 3.Oscillation in relation to through current



PACKAGE INFORMATION

Dimension in SOT-23 Package (Unit: mm)



SYMBOL	MIN	MAX
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.650	2.950
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

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